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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,091	09/17/2003	Danny Kenney	292609-605012	3730
41498	7590	11/02/2004		EXAMINER
RUDOLPH J. BUCHEL JR., LAW OFFICE OF P. O. BOX 702526 DALLAS, TX 75370-2526			LINDSAY JR, WALTER LEE	
			ART UNIT	PAPER NUMBER
			2812	

DATE MAILED: 11/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/664,091	KENNEY ET AL.
	Examiner	Art Unit
	Walter L. Lindsay, Jr.	2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on _____.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 11-20 is/are pending in the application.
 4a) Of the above claim(s) 20 is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 11-17 is/are rejected.
 7) Claim(s) 18 and 19 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input checked="" type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. <u>10/28/04</u> . |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

This Office Action is in response to an Election filed on 9/22/2004

Currently claims 11-20 are pending. Claims 1-10 are canceled.

Election/Restrictions

1. Applicant's election without traverse of claims 11-20 in the reply filed on 9/22/2004 is acknowledged.
2. Claims 1-10 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected method, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 9/22/2004.
3. Subsequently, claim 20 was withdrawn. See Examiner's Interview summary.

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

2. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

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Misnumbered claims the second claim 15 and claim 16 have been renumbered claim 16 and claim 17, respectively.

3. Claim 11 is objected to because of the following informalities: in lines 1-2 "reduced with soft error rates" should be "reduced soft error rates". Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 16 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 16 recites the limitation "said semiconductor" in line 4. There is insufficient antecedent basis for this limitation in the claim.

For examination purposes, "said semiconductor" will be treated as "said semiconductor substrate".

Additionally, it is suggested that line 2 of claim 16, be changed to read as follows: "the second dopant concentration is **further** based on a dopant concentration of said", in order to add clarity and to point out and distinctly claim the relationship between claim 16 and claim 13

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim 11 is rejected under 35 U.S.C. 102(e) as being anticipated by Hueting et al. (U. S. Patent No. 6,774,434, filed 11/12/2002).

Huetting shows the structure as claimed, in Figs. 1-2E and corresponding text, as: a semiconductor substrate (14) (Fig. 2A) (col. 8, lines 1-8); A first semiconductor layer (110) over the substrate, said first semiconductor layer being comprised of a first semiconductor material and having a vertical extent defined by an upper extent of the first semiconductor material and a lower extent of the first semiconductor material (col. 8, lines 8-10); a generally constant electric field across at least a portion (20) of the vertical extent of the first semiconductor material, wherein a charge which occurs within the first semiconductor layer is influenced toward the semiconductor substrate (Fig. 2D) (col. 7, lines 5-28)(col. 6, lines 8-10); and a device layer (110) in which a semiconductor device (30, 31, 32) may be fabricated (col. 8, lines 10-15) (claim 11). [The device layer is determined to be the layer in which the device is formed].

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huetting et al. (U. S. Patent No. 6, 774,434 filed 11/12/2002) in view of Clemens et al. (U.S. Patent No. 4,216,489 dated 8/5/1980).

Huetting shows the structure substantially as claimed and as described in the preceding paragraph.

Additionally, Huetting teaches that: the device layer is formed within the vertical extent of the first semiconductor material (110) (col. 8, lines 1-15) (claim 14).

Huetting lacks anticipation only in not explicitly teaching that: 1) the first semiconductor layer over the substrate further comprises a graded dopant concentration over at least a portion of the vertical extent of the first semiconductor

material, said graded dopant concentration having a first dopant concentration established at the lower extent of the semiconductor material, a second dopant concentration established at the upper extent of the semiconductor material, and a plurality of dopant concentrations between said first dopant concentration and said second dopant concentration over the at least a portion of the vertical extent of the first semiconductor material, and between the upper extent and lower extent of the first semiconductor material (claim 12); and 2) the second dopant concentration is based on the semiconductor device to be fabricated in the device layer (claim 13).

Clemens teaches a MOS device that implements bulk silicon and an epitaxial layer grown over the bulk silicon used to optimize dynamic memory device characteristics. Clemens teaches that an outdiffusion of dopants from the bulk semiconductor layer into the epitaxial layer exists and forms a graded dopant concentration that rapidly changes until the epitaxial layer reaches its desired value (col. 8, line 60-col. 9, line 8). The changes in dopant concentration allow for suppression of reverse-bias leakage current, and limit the availability of minority carriers, which does not lead to compromising desirable junction characteristics (col. 2, lines 24-32). The structure consequently has optimum capacitance, threshold and breakdown voltage characteristics, which lead to long hold times for individual memory cells (col. 4, lines 61-66).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the structure shown in Hueting, so that the first semiconductor material contains a graded dopant concentration, where a first dopant

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concentration at a lower portion and a second dopant concentration at an upper portion are established, with a plurality of dopant concentrations in between, and so that the second dopant concentration is based on the semiconductor device to be fabricated in the device layer, as taught by Clemens with the motivation, that Clemens teaches that a graded dopant concentration suppresses reverse-bias leakage current, and limits the availability of minority carriers, which prevents compromising desirable junction characteristics. Additional motivation is found in that Clemens teaches that the graded dopant concentration leads to optimum capacitance, and optimum threshold voltage characteristics, which lead to long hold times in memory cells.

11. Claim 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hueting et al. (U. S. Patent No. 6, 774,434 filed 11/12/2002) in view of Clemens et al. (U.S. Patent No. 4,216,489 dated 8/5/1980) as applied to claim 13 above, and further in view of Uyemura (copyrighted 1988 pp. 5-6).

Huetting as modified by Clemens shows the structure substantially as claimed and as described in the preceding paragraph.

Additionally Huetting as modified by Clemens shows that: the second dopant concentration is based on a dopant concentration of said semiconductor substrate, wherein said second dopant concentration is different from said dopant concentration of said semiconductor substrate (claim 15).

Huetting and Clemens lack anticipation only in not explicitly teaching that: 1) a second electric field formed at the lower extent of the first semiconductor material (claim

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15); and 2) the semiconducting structure comprises a second electric field below the first semiconductor material (claim 17).

Uyemura teaches that changes in the dopant concentration vary the intensity of the electric field (pp. 5-7).

It would be obvious to one of ordinary skill in the art, at the time the invention was made, to form a second electric field at the lower extent of the first semiconductor material, or a second electric field below the first semiconductor material according to the teachings of Huetting as modified by Clemens with the motivation that Uyemura teaches that variations of electric field occur with the change in dopant concentration, so that each dopant concentration level produces an individual electric field within the specific dopant concentration level that varies in intensity with another dopant concentration level.

Allowable Subject Matter

12. Claims 18-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

... an undoped intrinsic layer formed over said P+ semiconductor substrate and under said first semiconductor layer, as required by claim 18 as it depends from claim 17; and

... a buried n-layer formed over said P-semiconductor substrate; and
an undoped intrinsic layer formed over said buried n-layer and formed under said
first semiconductor layer, as required by claim 19, as it depends from claim 17.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John F Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL


October 26, 2004